WHAT IS CLAIMED IS:

1. A carrier for a semiconductor die package, the carrier comprising:

(a) a metal layer; and

(b) a plurality of bumps formed in the metal layer,

wherein the carrier is for electrically coupling a semiconductor die to a circuit substrate.

2. The carrier of claim 1 wherein the metal layer comprises copper.

3. The carrier of claim 1 wherein the plurality of bumps are disposed in an array and are stamped bumps.

4. The carrier of claim 1 further comprising:

a die attach region, and wherein the plurality of bumps are arranged around the die attach region.

5. The carrier of claim 1 further comprising a dielectric layer, wherein the metal layer is on a dielectric layer.

6. The carrier of claim 1 wherein the metal layer includes one or more sublayers of material on a base metal.

7. The carrier of claim 1 wherein the metal layer is discontinuous and includes a plurality of etched conductive lines that lead to the plurality of bumps.

8. The carrier of claim 1 wherein each bump has a conical angle of about 40 degrees of more.

9. The carrier of claim 1 wherein each bump has a conical shape.

10. A semiconductor die package comprising:

(a) a carrier comprising a metal layer, a die attach region, and a plurality of bumps formed in the metal layer; and

(b) a semiconductor die electrically coupled to the die attach region of the carrier.

11. The die package of claim 10 wherein the plurality of bumps are stamped bumps and are arranged around the die attach region, and wherein each of the bumps has a height that is greater than or equal to a thickness of the semiconductor die.

12. The die package of claim 10 wherein the carrier comprises copper.

13. The die package of claim 10 wherein the carrier comprises:
a base metal with one or more coatings on the base metal.

14. The die package of claim 10 wherein each bump has a conical angle greater than about 40 degrees.

15. The die package of claim 10 wherein the semiconductor die comprises a vertical metal oxide semiconductor field effect transistor (MOSFET) device.

16. The die package of claim 10 wherein the semiconductor die comprises a vertical metal oxide semiconductor field effect transistor (MOSFET) device having a source region, a gate region, and a drain region, wherein the drain region is proximate to the die attach region of the carrier, and the source region and the gate region are distal to the die attach region of the carrier.

17. The die package of claim 10 wherein each stamped bump has a conical shape.

18. The die package of claim 10 wherein the bumps and the semiconductor die are at opposite sides of the carrier.

19. The die package of claim 10 wherein the bumps and the semiconductor die are at the same side of the carrier.

20. A semiconductor die package comprising:

(a) a carrier comprising metal layer, a die attach region, and a plurality of stamped bumps formed in the metal layer around the die attach region;

(b) a semiconductor die comprising a vertical metal oxide semiconductor field effect transistor (MOSFET) device having a source region, a gate region, and a drain region, wherein the drain region is electrically coupled to and proximate to the die attach region of the carrier, and the source region and the gate region are distal to the die attach region, and wherein the plurality of stamped bumps in the carrier are arranged around the semiconductor die; and

(c) a plurality of solder deposits disposed on the semiconductor die.

21. The semiconductor die package of claim 20 wherein the each of the bumps has a conical angle greater than about 40 degrees or more.

22. The semiconductor die package of claim 20 wherein the carrier comprises copper.

23. The semiconductor die package of claim 20 the plurality of bumps are formed simultaneously in the metal layer.

24. A method for forming a carrier for a semiconductor die package, the method comprising:

(a) providing a metal layer; and

(b) forming a plurality of bumps in the metal layer, wherein the formed bumps are capable of being electrically coupled to conductive regions of a circuit substrate.

25. The method of claim 24 wherein forming the plurality of bumps comprises stamping.

26. A method for forming a semiconductor die package, the method comprising:

(a) forming a carrier according to the method of claim 24; and

(b) attaching a semiconductor die to the metal layer after forming the plurality of bumps.

27. The method of claim 26 wherein (c) attaching comprises:

attaching the semiconductor die to a die attach region of the carrier, and wherein the plurality of bumps is disposed around the semiconductor die.

28. The method of claim 26 wherein forming the plurality of bumps comprises stamping.